CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). A receiver circuit for a communications terminal, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a multiplexer for multiplexing the K digital signals ~~resulting in~~ and outputting at least one multiplexer output signal formed from the K multiplexed signals; and

a digital filter device for filtering the at least one multiplexer output signal ~~K multiplexed signals~~, said digital filter device having memory elements formed by shift registers of length K.

2-5 (canceled).

6 (previously presented). The receiver circuit according to claim 1, wherein said digital filter device has an order of magnitude L between 5 and 20.

7 (previously presented). The receiver circuit according to claim 1, wherein said digital filter device has an order of magnitude L between 10 and 18.

8 (previously presented). The receiver circuit according to claim 1, wherein said digital filter device includes:

a plurality of single digital filters; and

sampling rate reduction circuits that are configured in series in an alternating fashion.

9 (original) The receiver circuit according to claim 1, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal.

10 (original). The receiver circuit according to claim 1, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal into an in-phase reception signal and a quadrature reception signal.

11-12 (canceled).

13 (previously presented). The receiver circuit according to claim 1, wherein said signal-receiving device includes a plurality of reception sensors, each of said plurality of said reception sensors has a directional reception characteristic for sensing radio signals in a predefined spatial segment.

14 (canceled).

15 (currently amended). A mobile station of a mobile radio system, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a multiplexer for multiplexing the K digital signals ~~resulting in~~ and outputting at least one multiplexer output signal formed from the K multiplexed signals; and

a digital filter device for filtering the at least one multiplexer output signal ~~K multiplexed signals~~, said digital filter device having memory elements formed by shift registers of length K.

16-18 (canceled).

19 (currently amended). A receiver circuit for a communications terminal, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for

sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a stage containing K digital zero-inserting elements that are connected in parallel, each of said zero-inserting elements being fed with a respective one of the K digital signals and inserts K-1 zeros per sampling value of the respective one of the K digital signals ~~signal~~ into the respective one of the K digital signals ~~signal~~; and

a digital filter device for filtering the K digital signals ~~signal~~ with inserted zeros, said digital filter device having memory elements formed by shift registers of length K.

20 (previously presented). The receiver circuit according to claim 19, wherein said digital filter device has an order of magnitude L between 5 and 20.

21 (previously presented). The receiver circuit according to claim 19, wherein said digital filter device has an order of magnitude L between 10 and 18.

22 (previously presented). The receiver circuit according to claim 19, wherein said digital filter device includes:

a plurality of single digital filters; and

sampling rate reduction circuits that are configured in series in an alternating fashion.

23 (previously presented). The receiver circuit according to claim 19, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal.

24 (previously presented). The receiver circuit according to claim 19, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal into an in-phase reception signal and a

quadrature reception signal.

25 (previously presented). The receiver circuit according to claim 19, wherein said signal-receiving device includes a plurality of reception sensors, each of said plurality of said reception sensors has a directional reception characteristic for sensing radio signals in a predefined spatial segment.

26 (canceled).